REMARKS

The application has been carefully reviewed in light of the Final Office Action dated May 24, 2002. Claims 1-56 and 82-98 are pending in the application. Claims 38-56 are allowed. Applicant respectfully traverses the rejection. Favorable reconsideration is requested.

As previously explained, the present invention is an apparatus and method for adjusting clock skew. To reduce clock skew, a non-inverted clock signal ("CLK") and an inverted clock signal ("XCLK" – the complement) are connected to back-to-back inverters. The signal that takes longer to switch states (either CLK or XCLK) thus has an extra inverter driving it when it switches states and the signal that switches states faster has an extra inverter holding back the transition when it switches states. As a result, the "slower" signal (i.e., the one taking longer to switch states) and the "faster" signal are respectively altered relative to their transition times so that both signals effectively switch states at almost the same time (*see* specification page 12, lines 19 - page 14, lines 1-7; Fig. 4). The presently amended claims recite complementary clock signals, as well as the reduction in skew that results from the application of the presently claimed invention.

Claims 1-16, 26, 82-98 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which application regards as the invention. The Office Action states that "the recitation of claim calls for two inverters being configured as a latch . . . [the] function of

manipulating 'skew characteristic' cannot be carried out by a latch" (page 6 of Office Action). At the outset, applicant notes that the rejection is based on claim definiteness. There is nothing indefinite, in the rejected claims. Moreover, there is no technical support provided in the Office Action for the assertion that the defined invention cannot manipulate a skew characteristic. Indeed, the inverters defined in the claimed invention are not connected as a normal data latch, since each inverter receives a respective complementary phase clock signal. The Office Action assertion does not account for this. Moreover, the specification clearly explains in how the inverters affect the clock skew. The Office Action also erroneously declares that "transistors 60 and 64, in figure 3 . . provide skewing adjustment" (page 6 of Office action). The second paragraph of page 12 of the specification, cited by the Examiner, makes clear that transistors 60 and 64 only enable/disable the clock skew reduction circuit. In any event there is nothing indefinite in the claim language and withdrawal of this rejection is respectfully requested.

Claims 1-7, 16-19, 82 and 86-90 stand rejected under 35 U.S.C. §102(b) as being anticipated by *Makihara* et al. (US # 5,243,573). *Makihara* teaches a circuit that senses the logic level of data signals output from a memory array. Unlike the present invention, which receives two complementary clock signals as inputs, and adjusts them to reduce the skew between them, *Makihara* senses the difference between a data signal and a reference data signal and outputs the recognized signal and its complement on two output lines. No skew adjustment is conducted in the disclosed circuit. The portions cited in the Office Action (Fig. 2, etc.) discloses that the outputs N4 and N5 are being utilized to output a data signal and its complement (col. 2, lines 36-52; col. 3, lines 14-41); no input

27 are configured to receive complementary clock signals as inputs is simply incorrect. There is nothing in the disclosure of *Makihara* teaching or suggesting such a configuration.

The Office Action also states that the "voltage at node N4 [in *Makihara*] is seen to be swung between high voltage level (+V) and ground of the reference voltage generating circuit 10 which is controlled by element 21 by means of signal /BE as disclosed in figure 2 . . . therefore the signal provided at node N4 meets the definition of 'clock signal' as disclosed in the specification." This again is incorrect. The signal /BE is explicitly disclosed as a data signal (see FIG. 3). The specification in the present invention defines clock signals consistently as "signals that vary between a low voltage and a high voltage at regular intervals and are referenced to a fixed voltage, typically either the low voltage or the high voltage" (specification, page 1, lines 9-12). There are no "regular intervals" in which the data signal /BE switches from high to low; thus there is no way that /BE could be reasonably interpreted as a "clock signal". Accordingly, the rejection as to claims 1-7, 16-19, 82 and 86-90 is improper and should be withdrawn.

Claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Maikihara et al.* (US # 5,243,573) in view of *Garcia* (US # 5,949,259). *Garcia* does not teach or suggest the input of complementary clock signals, nor is there any disclosure of reducing skew rates within the clock signals. Thus, *Garcia* does not cure the deficiencies of *Makihara*. Accordingly, the rejections as to claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 are also improper and should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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